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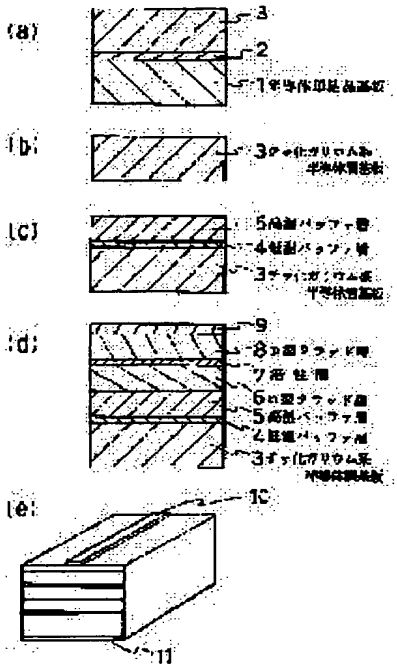
(54) MANUFACTURE OF SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PURPOSE: To provide a manufacturing method of a semiconductor light emitting lement wherein the generation of crystal defect and dislocation due to the mismatching of lattice constant and the difference of thermal expansion coefficients are restrained to the utmost, and cleavage is possible.
CONSTITUTION: This manufacturing method consists of the following; a proc ss wherein a gallium nitride based semiconductor layer 3 is formed on a semiconductor single crystal substrate 1, a process wherein the semiconductor single crystal substrate is eliminated, and a process wherein a gallium nitride based compound semiconductor single crystal layer containing at least an N-type layer and a P-type layer is further grown by eliminating a semiconductor crystal substrate and using the left gallium nitride based compound semiconductor layer as a new substrate.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] (a) The process of the semiconductor light emitting device which has the process which grows further the CHITSU-ized gallium system compound semiconductor single crystal layer which contains n type layer and p type layer at least by using as a new substrate the aforementioned CHITSU-ized gallium system compound semiconductor layer which r mov d and carried out the remainder of the process which forms a CHITSU-ized gallium system compound semiconductor layer, the process which removes the (b) aforementioned semiconductor single crystal substrate, and the (c) this semiconducting-crystal substrate on the semiconductor single crystal substrate.
[Claim 2] The aforementioned semiconductor single crystal substrate is the process of the semiconductor light emitting d vice according to claim 1 whose crystal face it is at least one sort of semiconductors chosen from the group which consists of GaAs, and GaP, InP and Si, and is the single crystal substrate of a field (111).
[Claim 3] The process of the semiconductor light emitting device according to claim 1 or 2 which forms membranes at th elevat d temperature of 700-1200 degrees C after forming the low-temperature buffer layer which consists the membrane formation process of the CHITSU-ized gallium system compound semiconductor layer of the aforementioned (a) process of a CHITSU-ized gallium system compound semiconductor layer at 400-700-degree C low temperature on the aforem ntioned semiconductor single crystal substrate.
[Claim 4] The process of the semiconductor light emitting device according to claim 1, 2, or 3 which forms the low-temperature buffer layer which consists of a CHITSU-ized gallium system compound semiconductor at 400-700-degree C low temp rature before growth of the CHITSU-ized gallium system compound semiconductor single crystal layer of the aforementioned (c) process, forms the elevated-temperature buffer layer which consists of a CHITSU-ized gallium system compound semiconductor at the elevated temperature of further 700-1200 degrees C, and grows the back aforementioned CHITSU-ized gallium system compound semiconductor single crystal layer.
[Claim 5] the above — the CHITSU-ized gallium system compound semiconductor single crystal layer which contains n type layer and p type layer even if few — n type clad layer — Have the sandwich structure of a barrier layer and p type clad layer, and the bandgap energy of this barrier layer constitutes each class of this sandwich structure from a semiconductor material smaller than the bandgap energy of this n type and p type clad layer. And the process of the semiconductor light emitting device according to claim 4 which forms this n type clad layer, p type clad layer, the afor mentioned elevated-temperature buffer layer, and the aforementioned CHITSU-ized gallium system compound s miconductor layer substrate by the semiconductor material of the same composition.
[Claim 6] The process of the semiconductor light emitting device according to claim 1 or 5 which chip-izes the s miconductor wafer with which the aforementioned CHITSU-ized gallium system compound semiconductor single crystal lay r was formed by the cleavage.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the process of a semiconductor light emitting device. It is related with the process of the semiconductor light emitting device using the still more detailed suitable CHITSU-ized gallium system compound semiconductor for blue luminescence.
[0002] A CHITSU-ized gallium system compound semiconductor is III here. The compound of Ga of a group element, and N of V group element, or III A part of Ga of a group element is other III(s), such as aluminum and In. The semiconductor which consists of a compound which a part of N of the thing replaced by the group element and/or V group element replaced by other V group elements, such as P and As, is said.
[0003] Moreover, a semiconductor light emitting device means the semiconductor device which generates light, such as light emitting diode (henceforth Light Emitting Diode) which has double heterojunctions, such as pn junction or pin, a superluminescent diode (SLD), or a semiconductor laser diode (LD).
[0004]
[Description of the Prior Art] Conventionally, by having obtained red and the p type semiconductor layer of low resistance which carried out the dopant of Mg, using a CHITSU-ized gallium system compound semiconductor in recent years although it compared green, and brightness is small and the difficulty was in utilization, brightness of blue Light Emitting Diode improves and it is basking in the limelight.
[0005] Light Emitting Diode of the conventional CHITSU-ized gallium system has structure as shown in drawing 5 . In order to manufacture this Light Emitting Diode, at 400-700-degree C low temperature to the sapphire (aluminum2 O3 single crystal) substrate 21 first An organometallic compound vapor growth It is carrier gas H2 by (it is hereafter called the MOCVD method). Trimethylgallium which is organometallic compound gas (It is hereafter called TMG), a trimethylaluminum (henceforth TMA), Trimethylindium (henceforth TMI) and ammonia (NH3) are supplied. About 0.01-0.2 micrometers of low-temperature buffer layers 22 which consist of Alx Gay In1-x-y (0<=x<1, 0< y<=1, x+y<=1) are formed. Subsequently, about 2-4 micrometers of elevated-temperature buffer layers 23 which supply the 700-1200-degree C same gas at an elevated temperature, and consist of Alx Gay In1-x-y N of n type of the same composition are formed.
[0006] Subsequently, the gas of the same ratio as the above-mentioned is supplied, about 0.1-0.3 micrometers of Alx Gay In1-x-y N layers 24 of n type of the same composition are formed, and n type clad layer for double heterojunction formation is formed. In order to form these n type layers, even if it does not dope n type impurity, in the case of a CHITSU-ized gallium system compound semiconductor, the property to become n type is used.
[0007] The barrier layer 25 which next consists of material Alp Gaq In1-p-q N (0 <=p<1, 0< q<=1, p+q<=1, p<x, 1-p-q> 1-x-y) to which the amount of aluminum is reduced from composition of a clad layer, the amount of In is made [many], and bandgap energy becomes small from that of a clad layer is formed.
[0008] Subsequently, the bis(cyclopentadienyl) magnesium for Mg or Zn as a p type impurity (henceforth Cp2 Mg) or the organometallic compound gas of dimethyl zinc (henceforth DMZn) is further added to the same material gas as formation of n type clad layer, it introduces into a coil, and p type clad layer 26 which consists of p type Alx Gay In1-x-y N is formed.
[0009] In order to consider as the cap layer 27 furthermore, the same gas as the above-mentioned is supplied, and the vapor growth of the p type AlxGay In1-x-y N layer is carried out.
[0010] after it and SiO2 etc. -- a protective coat is prepared all over the growth phase front face of a semiconductor, 400-800 degrees C and 20 - 60-minute room [about] annealing are performed, and activation of p type clad layer 26 which consists of p type Alx Gay In1-x-yN is attained Subsequently, dry etching according to chlorine plasma etc. in a part of each semiconductor layer which grew as patterning of the resist was applied and carried out and it was shown in drawing 5 , in order to form an n type electrode, after removing a protective coat is performed, and it is n type Alx. The Gay In1-x-y N layer 23 is exposed. Subsequently, metal membranes, such as Au and aluminum, are formed by sputtering etc., and the Light Emitting Diode chip is formed by forming and carrying out the dicing of the two electrodes 28 and 29.
[0011]
[Problem(s) to be Solved by the Invention] Since a rear-face side is an insulator in silicon on sapphire, in order that the semiconductor light emitting device using the conventional CHITSU-ized gallium system compound semiconductor may take the electrode by the side of a rear face, complicated processes, such as etching, are needed.
[0012] Moreover, although it is advantageously used since silicon on sapphire can bear an elevated temperature and can be doubled with the comparatively various crystal facs Fairly the lattice constant of silicon on sapphire and a CHITSU-ized gallium system semiconducting crystal by 4.758A and 3.189A, respectively Since it differs and coefficients of thermal expansion also differ further, As shown in A of drawing 6 , while transposition and a crystald fect occur in the buffer layer which touches silicon on sapphire, it progresses also to the CHITSU-ized gallium system compound semiconductor single crystal layer the crystal defect of whose is a layer of operation and an active region becomes narrow, there is a problem that the optical quality of a semiconductor layer also deteriorates.
[0013] Furthermore, the cleavage of the silicon on sapphire cannot be carried out, but with the above-mentioned structure, since a semiconductor light-emitting-device chip cannot be manufactured by the cleavage, there is a problem of being unsuitable in the device for which an end face needs two accurate parallel mirror plans like semiconductor laser.

[0014] this invention solves such a problem and it aims at offering the process of the semiconductor light emitting device which suppress d g nerating of a crystal def ct or transposition bas d on the mismatching of a lattice constant, or a differenc of a co fficient of thermal xpansion as much as possibl .
[0015] The purpose of further others of this inv ntion aims at off ring the process of the s miconductor light mitting device which can us a CHITSU-ized gallium system compound s miconductor also for th semiconductor light emitting device which n ds two mirror planes parallel to an end face like semiconductor las r, and can d al in the mirror plane of an nd fac by th cleavage.
[0016]
[Means for Solving th Probl m] Th proc ss to which the process of the semiconductor light mitting device of this inv ntion forms a CHITSU-ized gallium system compound semiconductor lay r on (a) s miconductor single crystal substrat , (b) The aforementioned CHITSU-ized gallium system compound semiconductor layer which removed and carried out the r mainder of the process which removes the aforementioned semiconductor single crystal substrate, and the (c) this semiconducting-crystal substrate is used as a new substrate. It has the process which grows further the CHITSU-ized gallium system compound semiconductor single crystal layer which contains n type layer and p type layer at least.
[0017] As for the aforementioned semiconductor single crystal substrate, it is desirable that it is at least one sort of semiconductors chosen from the group which consists of GaAs, and GaP, InP and Si, and the crystal face is the single crystal substrate of a field (111) from the point of the optical and the electrical property of the CHITSU-ized gallium syst m compound semiconductor layer formed on it.
[0018] Since forming membranes at the elevated temperature of 700-1200 degrees C becomes the buffer layer to which th afor mentioned low-temperature buffer layer softens mismatching with a substrate and it can prevent generating of a crystal d fect or transposition after forming the low-temperature buffer layer which consists the membrane formation proc ss of the CHITSU-ized gallium system compound semiconductor layer of the aforementioned (a) process of a CHITSU-ized gallium system compound semiconductor layer at 400-700-degree C low temperature on the aforementioned semiconductor substrate, it is desirable.
[0019] The low-temperature buffer layer which consists of a CHITSU-ized gallium system compound semiconductor at 400-700-degree C low temperature before growth of the CHITSU-ized gallium system compound semiconductor single crystal layer of the aforementioned (c) process is formed. The elevated-temperature buffer layer which consists of a CHITSU-ized gallium system compound semiconductor at the elevated temperature of further 700-1200 degrees C is form d. Since the influence of a crystal defect or dislocation whose thing to grow up produced the back aforemention d CHITSU-ized gallium system compound semiconductor single crystal layer in the CHITSU-ized gallium system compound s miconductor layer substrate can be suppressed to the minimum, it is desirable.
[0020] the above — the CHITSU-ized gallium system compound semiconductor single crystal layer which contains n type layer and p type layer even if few — n type clad layer — Have the sandwich structure of a barrier layer and p type clad layer, and the bandgap energy of this barrier layer constitutes each class of this sandwich structure from a semiconductor mat rial smaller than the bandgap energy of this n type and p type clad layer. And since the light emitting device of luminous fficiency with high forming this n type clad layer, p type clad layer, the aforementioned elevated-temperature buff r lay r, and the aforementioned CHITSU-ized gallium system compound semiconductor layer substrate by the semiconductor material of the same composition is obtained, it is desirable.
[0021] Since chip-izing the semiconductor wafer with which the aforementioned CHITSU-ized gallium system compound s miconductor single crystal layer was formed by the cleavage can mirror-plane-ize an end face, it is desirable.
[0022]
[Embodiments of the Invention] Below, the process of the semiconductor light emitting device of this invention is explained, r ferring to a drawing. It is cross-section explanatory drawing of the example of the semiconductor light emitting device by which drawing 1 was manufactured in process cross-section explanatory drawing of 1 operation form of the process of the s miconductor light emitting device of this invention, and drawing 2 -4 were manufactured by the process of this invention.
[0023] First, as shown in drawing 1 (a), the low-temperature buffer layer 2 and the elevated-temperature buffer layer 3 which become the front face of the semiconductor single crystal substrate 1 from a CHITSU-ized gallium system compound semiconductor layer by the MOCVD method are grown up.
[0024] As a semiconductor single crystal substrate 1, the crystal face can use the GaAs single crystal substrate which is a field, respectively (111), a GaP single crystal substrate, an InP single crystal substrate, or Si single crystal substrate, for example. The crystal face uses the semiconductor single crystal substrate of a field (111) because [of the crystal quality of a CHITSU-ized gallium system compound semiconductor layer]. Moreover, the above-mentioned semiconductor single crystal substrates, such as GaAs, are used because distortion by which a CHITSU-ized gallium system compound semiconductor, a lattice constant, etc. are comparatively applied to near and a CHITSU-ized gallium system compound s miconductor layer as compared with other materials can be made small.
[0025] Moreover, in order to grow up a semiconductor layer by the MOCVD method For arranging a substrate in a reactor and growing up the material gas for a vapor growth, for example, an Alx.Gay In1-x-y N layer, it is H2 of carrier gas. TMA which is organic-metal gas as material gas of aluminum, It is NH3 as material gas of TMI and N which are organic-metal gas as mat rial gas of TMG and In which are organic-metal gas as material gas of Ga. It introduces by each flow rate and is made to react in a furnace so that it may become a desired ratio. When growing up the semiconductor layer of different composition, th s miconductor lay r of desir d composition can be grown up by changing the introductory ratio, or introducing mat rial gas required for the l m nt of the composition, and making it react.
[0026] Although the growth temperature at th time of growing up a CHITSU-ized gallium system compound semiconductor is made to react at the elevated temp rature of 700-1200 degrees C to grow up a singl crystal and it is made to grow up About 0.01-0.2 micrometers of low-temperature buff r layers 2 grown up as a polycrystal film at 400-700-degree C low temperatur since the crystal ori ntation of a single crystal is not completely in agreement when making it grow up directly on the substrat of the dissimilar material from which a lattice constant etc. diff rs ar made to intervene. It is desirable to grow up the about 50-200-micrometer levat d-t mperature buffer layer 3 at the levated temperature of 700-1200 degr es C on it. In case this elevated-temperature buff r layer 3 is grown up, the low-temp rature buffer layer 2 which

grew as a polycrystal film at low temperature is also single-crystal-ized, and is adjustment-ized with the elevated-temp rature buffer layer 3.

[0027] As shown in drawing 1 (b) below, m chanical polish or chemical polish is carried out from the rear-face side of the semiconductor single crystal substrat 1, and the s miconducting-crystal substrat 1 and the low-t mp rature buffer layer 2 are remov d. The polish equipment which uses for example, diamond powder performs this mechanical polish, and the mixed liquor of a sulfuric acid and a hydrogen p roxide p rforms chemical polish.

[0028] As shown in drawing 1 (c) below, it arrang s in a r actor by using the elevated-t mperature buffer layer (CHITSU-iz d gallium system compound semiconductor layer) 3 which consists of a left-b hind CHITSU-ized gallium syst m compound s miconductor layer as a new substrate, and about 0.01-0.2 micrometers and about 1-40 micromet rs of elevat d-temperature buffer layers 5 are formed for the low-temp rature buffer layer 4 which consists of a CHITSU-ized gallium system compound semiconductor by the same method as the above-mentioned. Since the substrate which grows a CHITSU-ized gallium system compound semiconductor is a CHITSU-ized gallium system single crystal layer of the same kind, Although the CHITSU-ized gallium system compound semiconductor single crystal directly made into a following clad lay r and a following barrier layer without forming the low-temperature buffer layer 4 and the elevated-temperature buffer layer 5 may be grown up The CHITSU-ized gallium system compound semiconductor layer substrate 3 newly used as a substrate here is what was formed on the semiconducting-crystal substrate 1 of a different kind. The crystal defect and dislocation based on grid mismatching may have occurred, and a crystal defect and dislocation may progress also to the CHITSU-ized gallium system compound semiconductor single crystal layer formed on it in that case. Therefore, it is desirabl to form the low-temperature buffer layer 4 and the elevated-temperature buffer layer 5 again. The growth method of this low-temperature buffer layer 4 and the elevated-temperature buffer layer 5, the use, etc. are the same as that of the low-t mperature buffer layer 2 of drawing 1 (a), and the elevated-temperature buffer layer (CHITSU-ized gallium system compound semiconductor layer substrate) 3.

[0029] As shown in drawing 1 (d) below, n type clad layer 6, a non dope, n type or the p type barrier layer 7, p type clad layer 8, and the cap layer 9 are formed one by one. The clad layers 6 and 8 are usually formed in the thickness of about 0.1-2 micrometers, and a barrier layer 7 is formed in the thickness of about 0.05-0.1 micrometers. Although a barrier layer 7 is formed in the grade which neither a crystal defect nor dislocation cannot generate very thinly, it is desirable that a limitation is to make a clad layer thin, distortion will tend to enter if these consist of dissimilar materials, since it is thick, and a thick layer is formed with the material of the same composition with the elevated-temperature buffer layer 5.

[0030] in order to make it n type layer in semiconductor layers, such as the above-mentioned clad layer, — Si, germanium, and Sn — SiH4, GeH4, and SnH4 etc. — it is obtained by mixing in reactant gas as gas Moreover, in order to form p type layer, it can consider as p type layer by mixing Mg and Zn in material gas as Cp2 Mg or organic-metal gas of DMZn. this p typ layer — the cap layer 9 top — SiO2 etc. — from — preparing the becoming protective coat and carrying out ann aling processing at 400-800 degrees C, or by irradiating an electron ray, H (H of NH3 gas which is H2 and reactant gas as carri r gas combines) combined with Mg is separated, it can be made easy to move and Mg can be formed into low resistance

[0031] In this example, it considers as the double heterojunction structure which sandwiches the both sides of a barrier layer 7 by both the clad layers 6 and 8 of p type layer and n type layer, and the clad layers 6 and 8 consist of material which has bigger bandgap energy than the bandgap energy of a barrier layer 7. In order to enlarge bandgap energy with the material of the above-mentioned Alx Gay In1-x-y N, it is obtained by enlarging x and making 1-x-y small. since the carrier pour d into the barrier layer by considering as a sandwich structure in the clad layers 6 and 8 which have such bandgap nergy is shut up in the energy barrier made between the barrier layer which is a luminous layer, and a clad layer, from the homozygous structure which made pn junction from the same simple material, establishment of radiative recombination is mark dly alike, and improves, and luminous efficiency also becomes high However, the process of this invention is similarly appli d only by changing composition of the semiconductor layer it is not limited to such double heterojunction structure, and th pn junction of homozygous or a heterojunction also grows up to be. Moreover, the semiconductor light emitting d vic made into refractive-index waveguide structure can be similarly manufactured by forming a stripe slot by s miconductor laser. In addition, the cap layer 9 is a thing for the fall of contact resistance with the electrode metal 10, and is form d in the thickness of about 0.2 micrometers or less.

[0032] Electron beam irradiation is carried out by about 3-20kV acceleration voltage from a direct front face without preparing protective coats, such as SiO2, Si 3N4, and aluminum 2O3, in the front face of a semiconductor layer, performing annealing processing of a 20 - 60-minute about room at 400-800 degrees C or preparing a protective coat as mentioned above n xt. Consequently, junction to Mg and H which are the dopant of p type layer is cut, activation is attained, and low resistance-ization of p type layer is attained.

[0033] Subsequently, in order that electrode materials, such as Au and aluminum, may be formed by vacuum evaporationo, the spatter, etc., the lower (n side) electrode 11 may be formed in the whole surface at a rear-face side and a front-face side may secure a luminescence field in the case of Light Emitting Diode, Or in order to regulate a current pouring field in the cas of semiconductor laser, patterning is carried out, the up (p side) electrode 10 is formed so that it may remain only in a cor , and as shown to drawing 1 (e) in a perspective diagram, a semiconductor light-emitting-device chip is formed by carrying out a cleavage to after each chip.

[0034] After Light Emitting Diode lays and carries out wirebonding of the chip to a stem again by carrying out a mould by the epoxy resin after laying and carrying out wir bonding of this semiconductor light- mitting-device chip to a l adframe, a laser diode is completed by carrying out a seal with a cap.

[0035] Since according to this invention a semiconductor single crystal substrate is removed and the CHITSU-ized gallium system compound semiconductor single crystal layer of a layer of operation is grown up on it by using a CHITSU-ized gallium system compound semiconductor layer as a n w substrate after growing up a CHITSU-ized gallium system compound semiconductor layer on a semiconductor single crystal substrate, a lattice constant and a coeffici nt of thermal expansion become very near, and it is hard to generate a lattice defect and dislocation.

[0036] A crystal defect occurs in the CHITSU-ized gallium system compound semiconductor layer which originates in the grid mismatching between the CHITSU-iz d gallium system compound semiconductor lay rs and semiconductor single

crystal substrat s which ar used as the new substrat grown up on the semiconductor singl crystal substrate on the other hand, and is us d as a n w substrat . It spr ads to th CHITSU-iz d gallium system compound semiconductor single crystal layer which the crystal defect uses as a layer of operation, and although we are anxious about dislocation and a crystal defect occurring, about the dislocation and def ct, it can pr vent effectively by pr paring a low-temperature buffer lay r and an levat d-t mperature buffer layer b tween them.

[0037] Furthermore, a mirror plan becomes a beautiful cleavage plane is obtained and is easy to b obtained by making the same composition of th semiconductor singl crystal layer of the lay r thickly formed in 1 microm ters or more of a buffer layer and a clad layer.

[0038] Below, a still more concrete light emitting device xplains th process of this inv ntion in detail.

[0039]

[Exampl]

Example 1 drawing 2 is cross-section explanatory drawing of CHITSU-ized gallium system double heterojunction Light Emitting Diode manufactured by the process of this invention. A double heterojunction is formed by changing the ratio of aluminum, Ga, and In, using Alx Gay In1-x-y N (0<=x<1, 0< y<=1, 0<x+y<=1) as a CHITSU-ized gallium system compound semiconductor.

[0040] first On the front face of the CHITSU-ized gallium system compound semiconductor layer substrate 3 used as the new substrate which consists of a semiconductor layer of n type Alx Gay In1-x-y N formed in the thickness of 50-200 micromet rs as shown in above-mentioned drawing 1 (b), at 400-700-degree C low temperature n type AlvGaw In1-v-w N (v<=x 0<=v<1, 0< w<=1, and 0<v+w<=1 —) About 0.01-0.2 micrometers grows the low-temperature buffer layer 4 which consists of 1-x-y<=1-v-w by the MOCVD method. Subsequently, the elevated-temperature buffer layer 5 which consists of n type Alx GayIn1-x-y N of the same composition as the CHITSU-ized gallium system compound semiconductor layer substrat 3 at the elevated temperature of 700-1200 degrees C was formed in the thickness of about 1-40 micrometers. n typ clad layer 6 which consists of n type Alx Gay In1-x-y N at further 700-1200 degrees C is formed in the thickness of about 0.1-2 micrometers. Alp Gaq In1-p-q N (p<x 0<=p<1, 0< q<=1, and 0<p+q<=1 —) of a non dope The barrier layer 7 which consists of 1-p-q>1-x-y was grown up into the thickness of about 0.05-0.1 micrometers, and 1-2 micrometers of p type clad layers 8 which consist of p type Alx Gay In1-x-yN further were grown up. The cap layer 9 which consists of Alr Gas In1-r-s N (0<=r<1, 0< s<=1, 0<r+s<=1, r<=x, 1-x-y<=1-r-s) on it is formed in about 0.2-micrometer thickness.

[0041] With the aforementioned structure, both the clad layers 6 and 8 are the same composition, and these layers are formed with composition with large bandgap energy from composition of a barrier layer 7. That is, by making [many] the amount of aluminum and lessening the amount of In, a large material of bandgap energy is obtained, it has the structure where the barrier layer 7 which bandgap energy becomes from a small material by the clad layers 6 and 8 which consist of a large material of bandgap energy is sandwiched, the carrier poured into the barrier layer is shut up in an energy barrier, and luminous efficiency is made high.

[0042] Low resistance-ization of p type layer was attained by electron beam irradiation as mentioned above the back, and blue Light Emitting Diode of the double heterojunction of the brightness about 0.5 cd (cd) was obtained by forming and carrying out the cleavage of the electrode.

[0043] Since it is considering as the double heterojunction which makes a sandwich structure the barrier layer which consists of a small material of bandgap energy according to this example, while being able to raise luminous efficiency, thick semiconductor layers, such as a clad layer and a buffer layer, constitute from material of the same composition, since the s miconductor layer of different composition is formed in the thinness which is the grade which a crystal defect does not produce, the semiconductor layer which was excellent in membraneous quality without a defect is obtained, and it becomes still easi r [a cleavage].

[0044] Example 2 this example is an example of a semiconductor laser type light emitting device, and formation of each class and formation of an electrode form completely like an example 1, ********** the upper part of the cap layer 9 of the both sides of the up electrode 11, and p type clad layer 8 after electrode formation, and it makes them a mesa type configuration. Since with such structure current was able to be centralized only on the core of a barrier layer and the end face was moreover a mirror plane by the cleavage, it could be made to be able to reflect by the end face, and could be made to oscillate, and the blue semiconductor laser type light emitting device whose output is about 0.2mW was obtained.

[0045] The low-temperature buffer layer 4 which example 3 this example is an example of Light Emitting Diode of pn junction, and becomes the CHITSU-ized gallium system compound semiconductor layer substrate 3 from n type GaN About 0.01-0.2 micrometers, The elevated-temperature buffer layer 5 which consists of n type GaN is grown up on the conditions as an xample 1 that only the thickness of about 1-40 micrometers is the same. n type layer 12 which consists of n mold Alt Ga1-t N (0<=t<1) the back About 1-2 micrometers, p type layer 13 which consists of p mold Inu Ga1-u N (0<=u<1) About 0.1-0.3 micrometers, Form membranes, respectively and the cap layer 14 which subsequently consists of p mold Alz Ga1-z N (0<=z<1) is formed. After making electron beam irradiation p type layer 13 by about 3-20kV acceleration voltage and performing annealing, the lower (n side) electrode 11 and the up (p side) electrode 10 were formed, and pn junction Light Emitting Diode of a heterojunction was manufactured. By considering as this heterojunction structure, luminous efficiency increased and blue Light Emitting Diode of the brightness which is a 0.2-cd (cd) grade was obtained.

[0046]

[Effect of the Invention] Since a substrate is not an insulating substrate, according to this invention, it is not necessary to ********** from an upper surface side lik before, to xpose a lower conductivity-type layer that what is necessary is just to form the l ctrode by th side of the lower part in the rear face of a substrate, and to form an l ctrode. Therefore, while a dry etching process becomes unnecessary and a structure process becomes easy, property degradation which originates in resistanc by the contamination which is asy to generate at the time of etching is not produced, either.

[0047] Furthermor , since the substrate also consists of the same CHITSU-iz d gallium system compound semiconductor lay r as a layer with a thick clad layer etc., a crystal of the same kind can gather, a cleavage can be carried out easily, and it can d al in a mirror plane asily. Consequently, it can deal also in blue semiconductor laser easily.

[0048] Moreover, sinc th substrate also consists of a CHITSU-ized gallium system compound semiconductor layer, it is a layer of operation and a semiconductor layer of the same kind, and a lattice constant etc. can be in agreement, grid

adjustment can be taken, and generating of a crystal defect or transposition can be prevented. Consequently, a semiconductor layer b comes quality and the luminous efficiency and th life of an element improve.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Bri f Description of the Drawings]
[Drawing 1] It is drawing showing the manufacturing process of 1 operation gestalt of the process of the semiconductor light mitting device of this invention.
[Drawing 2] It is cross-section explanatory drawing of Light Emitting Diode manufactured according to one example of the process of this invention.
[Drawing 3] It is cross-section explanatory drawing of the semiconductor laser manufactured according to other exampl s of th process of this invention.
[Drawing 4] It is cross-section explanatory drawing of Light Emitting Diode manufactured according to the example of furth r others of the process of this invention.
[Drawing 5] It is cross-section explanatory drawing of the conventional GaN system Light Emitting Diode.
[Drawing 6] It is drawing explaining the situation of the transposition generated in the buffer layer formed on conventional silicon on sapphire.
[Description of Notations]
1 S miconductor Single Crystal Substrate
3 CHITSU-ized Gallium System Compound Semiconductor Layer Substrate
4 Low-t mperature Buffer Layer
5 El vat d-Temperature Buffer Layer
6 N Typ Clad Layer
7 Barri r Layer
8 P Typ Clad Layer

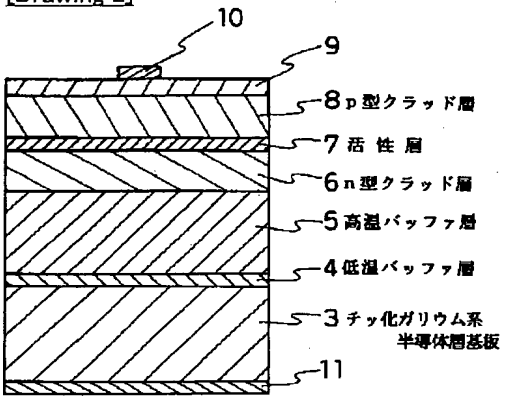
[Translation done.]

* NOTICES *

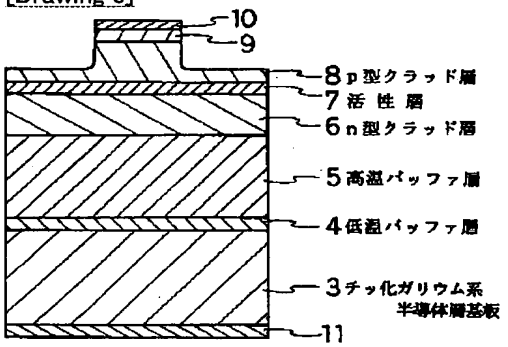
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

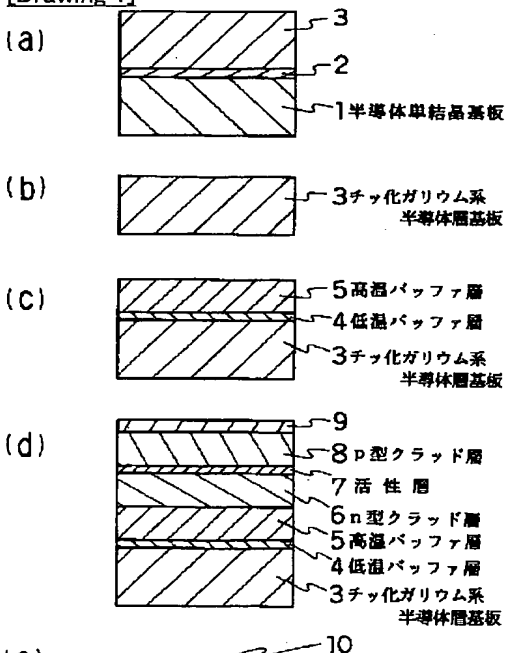
[Drawing 2]



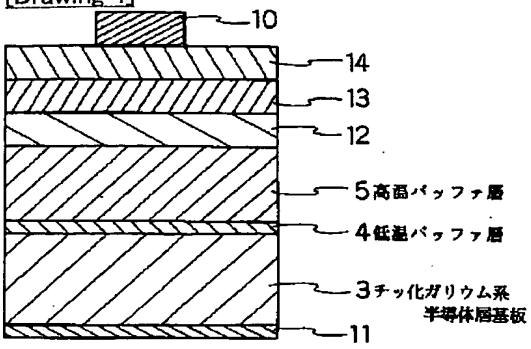
[Drawing 3]



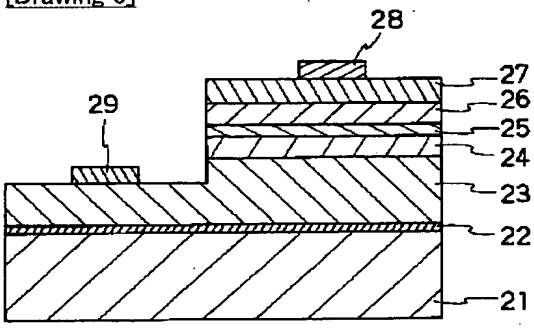
[Drawing 1]



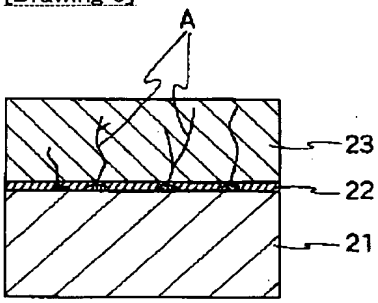
[Drawing 4]



[Drawing 5]



[Drawing 6]



[Translation done.]

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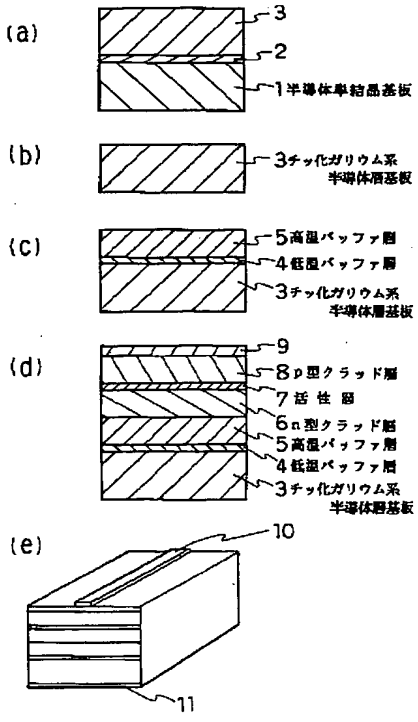
(54)【発明の名称】半導体発光素子の製法

(57)【要約】

【課題】　格子定数の不整合や熱膨張係数の相違に基づく結晶欠陥や転位の発生を極力抑え、かつ、劈開することができる半導体発光素子の製法を提供する。

【解決手段】　（ａ）半導体単結晶基板１上にチッ化ガウリウム系半導体層３を成膜する工程、（ｂ）前記半導体単結晶基板を除去する工程、および（ｃ）該半導体結晶基板を除去して残余した前記チッ化ガリウム系化合物半導体層を新たな基板として、少なくともｎ型層およびｐ型層を含むチッ化ガリウム系化合物半導体単結晶層をさらに成長する工程を有する。



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【特許請求の範囲】

【請求項１】　（ａ）半導体単結晶基板上にチッ化ガリウム系化合物半導体層を成膜する工程、（ｂ）前記半導体単結晶基板を除去する工程、および（ｃ）該半導体結晶基板を除去して残余した前記チッ化ガリウム系化合物半導体層を新たな基板として、少なくともｎ型層およびｐ型層を含むチッ化ガリウム系化合物半導体単結晶層をさらに成長する工程を有する半導体発光素子の製法。

【請求項２】　前記半導体単結晶基板は、ＧａＡｓ、ＧａＰ、ＩｎＰおよびＳｉよりなる群から選ばれた少なくとも１種の半導体で、かつ、結晶面が（１１１）面の単結晶基板である請求項１記載の半導体発光素子の製法。

【請求項３】　前記（ａ）工程のチッ化ガリウム系化合物半導体層の成膜工程を、前記半導体単結晶基板上に４００～７００℃の低温でチッ化ガリウム系化合物半導体層からなる低温バッファ層を形成したのちに７００～１２００℃の高温で成膜する請求項１または２記載の半導体発光素子の製法。

【請求項４】　前記（ｃ）工程のチッ化ガリウム系化合物半導体単結晶層の成長前に４００～７００℃の低温でチッ化ガリウム系化合物半導体からなる低温バッファ層を成膜し、さらに７００～１２００℃の高温でチッ化ガリウム系化合物半導体からなる高温バッファ層を成膜し、そののち前記チッ化ガリウム系化合物半導体単結晶層を成長する請求項１、２または３記載の半導体発光素子の製法。

【請求項５】　前記少なくともｎ型層およびｐ型層を含むチッ化ガリウム系化合物半導体単結晶層がｎ型クラッド層、活性層、ｐ型クラッド層のサンドイッチ構造を有し、該サンドイッチ構造の各層は該活性層のバンドギャップエネルギーが該ｎ型およびｐ型クラッド層のバンドギャップエネルギーより小さい半導体材料で構成し、かつ、該ｎ型クラッド層、ｐ型クラッド層、前記高温バッファ層および前記チッ化ガリウム系化合物半導体層基板を同一組成の半導体材料で形成する請求項４記載の半導体発光素子の製法。

【請求項６】　前記チッ化ガリウム系化合物半導体単結晶層が形成された半導体ウェハを劈開によりチップ化する請求項１または５記載の半導体発光素子の製法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体発光素子の製法に関する。さらに詳しくは、青色発光に好適なチッ化ガリウム系化合物半導体を用いた半導体発光素子の製法に関する。

【０００２】ここにチッ化ガリウム系化合物半導体とは、III 族元素のＧａとＶ族元素のＮとの化合物またはIII 族元素のＧａの一部がＡｌ、Ｉｎなど他のIII 族元素と置換したものおよび／またはＶ族元素のＮの一部がＰ、Ａｓなど他のＶ族元素と置換した化合物からなる半導体をいう。

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【０００３】また、半導体発光素子とは、ｐｎ接合またはｐｉｎなどダブルヘテロ接合を有する発光ダイオード（以下、ＬＥＤという）、スーパルミネッセントダイオード（ＳＬＤ）または半導体レーザダイオード（ＬＤ）などの光を発生する半導体素子をいう。

【０００４】

【従来の技術】従来青色のＬＥＤは赤色や緑色に比べて輝度が小さく実用化に難点があったが、近年チッ化ガリウム系化合物半導体を用い、Ｍｇをドーパントした低抵抗のｐ型半導体層がえられたことにより、輝度が向上し脚光をあびている。

【０００５】従来のチッ化ガリウム系のＬＥＤは、たとえば図５に示されるような構造になっている。このＬＥＤを製造するには、まずサファイア（Al_2O_3 単結晶）基板２１に４００～７００℃の低温で有機金属化合物気相成長法（以下、ＭＯＣＶＤ法という）によりキャリアガスH_2 とともに有機金属化合物ガスであるトリメチルガリウム（以下、ＴＭＧという）、トリメチルアルミニウム（以下、ＴＭＡという）、トリメチルインジウム（以下、ＴＭＩという）およびアンモニア（NH_3）を供給し、$Al_xGa_yIn_{1-x-y}$（$0 \leqq x < 1$、$0 < y \leqq 1$、$x+y \leqq 1$）からなる低温バッファ層２２を０．０１～０．２μｍ程度形成し、ついで７００～１２００℃の高温で同じガスを供給し同じ組成のｎ型の$Al_xGa_yIn_{1-x-y}N$からなる高温バッファ層２３を２～４μｍ程度形成する。

【０００６】ついで前述と同じ比率のガスを供給して同じ組成のｎ型の$Al_xGa_yIn_{1-x-y}N$層２４を０．１～０．３μｍ程度形成し、ダブルヘテロ接合形成のためのｎ型クラッド層を形成する。これらのｎ型層を形成するには、チッ化ガリウム系化合物半導体のばあい、ｎ型不純物をドープしなくてもｎ型になるという性質を利用している。

【０００７】つぎに、クラッド層の組成よりＡｌの量を減らしＩｎの量を多くしてバンドギャップエネルギーがクラッド層のそれより小さくなる材料$Al_pGa_qIn_{1-p-q}N$（$0 \leqq p < 1$、$0 < q \leqq 1$、$p+q \leqq 1$、$p < x$、$1-p-q > 1-x-y$）からなる活性層２５を形成する。

【０００８】ついで、ｎ型クラッド層の形成と同じ原料ガスにさらにｐ型不純物としてのＭｇまたはＺｎのためのビスシクロペンタジエニルマグネシウム（以下、Cp_2Mgという）またはジメチル亜鉛（以下、ＤＭＺｎという）の有機金属化合物ガスを加えて反応管に導入し、ｐ型$Al_xGa_yIn_{1-x-y}N$からなるｐ型クラッド層２６を形成する。

【０００９】さらにキャップ層２７とするため、前述と同様のガスを供給してｐ型の$Al_xGa_yIn_{1-x-y}N$層を気相成長させる。

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【００１０】そののち、SiO_2などの保護膜を半導体の成長層表面全面に設け、４００～８００℃、２０～６０分間程度のアニールを行い、ｐ型$Al_xGa_yIn_{1-x-y}N$からなるｐ型クラッド層２６の活性化を図る。ついで保護膜を除去したのちｎ型の電極を形成するため、レジストを塗布しパターニングして、図５に示されるように、成長した各半導体層の一部を塩素プラズマなどによるドライエッチングを行ってｎ型$Al_xGa_yIn_{1-x-y}N$層２３を露出させる。ついでＡｕ、Ａｌなどの金属膜をスパッタリングなどにより形成して両電極２８、２９を形成し、ダイシングすることによりＬＥＤチップを形成している。

【００１１】

【発明が解決しようとする課題】従来のチッ化ガリウム系化合物半導体を用いた半導体発光素子は裏面側がサファイア基板で絶縁体であるため、裏面側の電極をとるためにエッチングなどの複雑なプロセスが必要となる。

【００１２】また、サファイア基板は高温に耐えることができ、比較的種々の結晶面に合わせることができるため有利に用いられているが、サファイア基板とチッ化ガリウム系半導体結晶との格子定数はそれぞれ４．７５８Åと３．１８９Åで相当異なり、さらに熱膨脹係数も異なるため、図６のＡに示されるように、サファイア基板と接するバッファ層に転位や結晶欠陥が発生し、その結晶欠陥が動作層であるチッ化ガリウム系化合物半導体単結晶層にも進展し動作領域が狭くなるとともに、半導体層の光学的品質も低下するという問題がある。

【００１３】さらに、サファイア基板を劈開することはできず、前述の構造では劈開により半導体発光素子チップを製造することができないため、半導体レーザのように端面が精度のよい平行な２つの鏡面を必要とするデバイスには不向きであるという問題がある。

【００１４】本発明はこのような問題を解決し、格子定数の不整合や熱膨脹係数の相違に基づく結晶欠陥や転位の発生を極力抑えた半導体発光素子の製法を提供することを目的とする。

【００１５】本発明のさらに他の目的は半導体レーザのように端面に平行な２つの鏡面を必要とする半導体発光素子にもチッ化ガリウム系化合物半導体を用いて劈開により端面の鏡面をうることができる半導体発光素子の製法を提供することを目的とする。

【００１６】

【課題を解決するための手段】本発明の半導体発光素子の製法は、（ａ）半導体単結晶基板上にチッ化ガリウム系化合物半導体層を成膜する工程、（ｂ）前記半導体単結晶基板を除去する工程、および（ｃ）該半導体結晶基板を除去して残余した前記チッ化ガリウム系化合物半導体層を新たな基板として、少なくともｎ型層およびｐ型層を含むチッ化ガリウム系化合物半導体単結晶層をさらに成長する工程を有する。

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【００１７】前記半導体単結晶基板は、ＧａＡｓ、ＧａＰ、ＩｎＰおよびＳｉよりなる群から選ばれた少なくとも１種の半導体で、かつ、結晶面が（１１１）面の単結晶基板であることが、その上に形成されるチッ化ガリウム系化合物半導体層の光学的および電気的特性の点から好ましい。

【００１８】前記（ａ）工程のチッ化ガリウム系化合物半導体層の成膜工程を、前記半導体基板上に４００～７００℃の低温でチッ化ガリウム系化合物半導体層からなる低温バッファ層を形成したのちに７００～１２００℃の高温で成膜することが、前記低温バッファ層が基板との不整合を和らげるバッファ層となり、結晶欠陥や転位の発生を防止できるため好ましい。

【００１９】前記（ｃ）工程のチッ化ガリウム系化合物半導体単結晶層の成長前に４００～７００℃の低温でチッ化ガリウム系化合物半導体からなる低温バッファ層を成膜し、さらに７００～１２００℃の高温でチッ化ガリウム系化合物半導体からなる高温バッファ層を成膜し、そののち前記チッ化ガリウム系化合物半導体単結晶層を成長することが、チッ化ガリウム系化合物半導体層基板に生じた結晶欠陥や転位の影響を最小限に抑制することができるため好ましい。

【００２０】前記少なくともｎ型層およびｐ型層を含むチッ化ガリウム系化合物半導体単結晶層がｎ型クラッド層、活性層、ｐ型クラッド層のサンドイッチ構造を有し、該サンドイッチ構造の各層は該活性層のバンドギャップエネルギーが該ｎ型およびｐ型クラッド層のバンドギャップエネルギーより小さい半導体材料で構成し、かつ、該ｎ型クラッド層、ｐ型クラッド層、前記高温バッファ層および前記チッ化ガリウム系化合物半導体層基板を同一組成の半導体材料で形成することが、発光効率の高い発光素子がえられるため好ましい。

【００２１】前記チッ化ガリウム系化合物半導体単結晶層が形成された半導体ウェハを劈開によりチップ化することが、端面を鏡面化することができるため好ましい。

【００２２】

【発明の実施の形態】つぎに、図面を参照しながら本発明の半導体発光素子の製法について説明する。図１は本発明の半導体発光素子の製法の一実施形態の工程断面説明図、図２～４は本発明の製法により製造された半導体発光素子の例の断面説明図である。

【００２３】まず、図１（ａ）に示されるように、半導体単結晶基板１の表面にＭＯＣＶＤ法によりチッ化ガリウム系化合物半導体層からなる低温バッファ層２および高温バッファ層３を成長する。

【００２４】半導体単結晶基板１としては、たとえば結晶面がそれぞれ（１１１）面であるＧａＡｓ単結晶基板、ＧａＰ単結晶基板、ＩｎＰ単結晶基板またはＳｉ単結晶基板を使用することができる。結晶面が（１１１）面の半導体単結晶基板を使用するのは、チッ化ガリウム

系化合物半導体層の結晶品質のためである。またＧａＡｓなど前述の半導体単結晶基板を使用するのは、他の材料と比較してチッ化ガリウム系化合物半導体と格子定数などが比較的近く、チッ化ガリウム系化合物半導体層にかかる歪を小さくできるためである。

【００２５】またＭＯＣＶＤ法により半導体層を成長させるには、反応炉内に基板を配設し、気相成長のための原料ガス、たとえば$Al_xGa_yIn_{1-x-y}N$層を成長させるにはキャリアガスのH_2にＡｌの原料ガスとして有機金属ガスであるＴＭＡ、Ｇａの原料ガスとして有機金属ガスであるＴＭＧ、Ｉｎの原料ガスとして有機金属ガスであるＴＭＩ、およびＮの原料ガスとしてNH_3を所望の比率になるようにそれぞれの流量で導入して炉内で反応させる。異なる組成の半導体層を成長させるばあいは、その導入比率を変えたり、またはその組成の元素に必要な原料ガスを導入して反応させることにより所望の組成の半導体層を成長させることができる。

【００２６】チッ化ガリウム系化合物半導体を成長させる際の成長温度は単結晶を成長させるには７００～１２００℃の高温で反応させて成長させるが、格子定数などが異なる異種材料の基板上に直接成長させるばあいは完全には単結晶の結晶方向が一致しないため４００～７００℃の低温で多結晶膜として成長させる低温バッファ層２を０．０１～０．２μｍ程度介在させ、その上に７００～１２００℃の高温で５０～２００μｍ程度の高温バッファ層３を成長させることが好ましい。この高温バッファ層３を成長させる際に低温で多結晶膜として成長した低温バッファ層２も単結晶化し、高温バッファ層３と整合化される。

【００２７】つぎに図１（ｂ）に示されるように、半導体単結晶基板１の裏面側から機械的研磨または化学的研磨をし、半導体結晶基板１および低温バッファ層２を除去する。この機械的研磨は、たとえばダイヤモンド粉を使用する研磨装置により行い、化学的研磨は、たとえば硫酸と過酸化水素の混合液により行う。

【００２８】つぎに図１（ｃ）に示されるように、残されたチッ化ガリウム系化合物半導体層からなる高温バッファ層（チッ化ガリウム系化合物半導体層）３を新たな基板として反応炉内に配設し、前述と同様の方法でチッ化ガリウム系化合物半導体からなる低温バッファ層４を０．０１～０．２μｍ程度、高温バッファ層５を１～４０μｍ程度設ける。チッ化ガリウム系化合物半導体を成長する基板は同種のチッ化ガリウム系単結晶層であるため、低温バッファ層４および高温バッファ層５を設けないで直接つぎのクラッド層や活性層とするチッ化ガリウム系化合物半導体単結晶を成長させてもよいが、ここで新たに基板とするチッ化ガリウム系化合物半導体層基板３は異種の半導体結晶基板１上に形成されたもので、格子不整合に基づく結晶欠陥や転位が発生している可能性があり、そのばあい、その上に成膜されるチッ化ガリウム系化合物半導体単結晶層にも結晶欠陥や転位が進む可能性がある。そのため、再度低温バッファ層４および高温バッファ層５を設けることが好ましい。この低温バッファ層４および高温バッファ層５の成長方法や効用などは図１（ａ）の低温バッファ層２および高温バッファ層（チッ化ガリウム系化合物半導体層基板）３と同様である。

【００２９】つぎに図１（ｄ）に示されるように、ｎ型クラッド層６、ノンドープまたはｎ型もしくはｐ型の活性層７、ｐ型クラッド層８、キャップ層９を順次形成する。クラッド層６、８は通常０．１～２μｍ程度の厚さに形成され、活性層７は０．０５～０．１μｍ程度の厚さに形成される。活性層７は結晶欠陥や転位が発生しえない程度に非常に薄く形成されるが、クラッド層は薄くするのに限界があり、厚いため、これらが異種材料で構成されると歪みが入り易く、高温バッファ層５とともに厚い層は同じ組成の材料で形成されることが好ましい。

【００３０】前述のクラッド層などの半導体層でｎ型層にするためには、Ｓｉ、Ｇｅ、ＳｎをＳｉH_4、ＧｅH_4、ＳｎH_4などのガスとして反応ガス内に混入することによりえられる。またｐ型層を形成するためには、ＭｇやＺｎをCp_2ＭｇやＤＭＺｎの有機金属ガスとして原料ガスに混入することによりｐ型層とすることができる。このｐ型層はキャップ層９上にSiO_2などからなる保護膜を設けて４００～８００℃でアニール処理をすることにより、または電子線を照射することによりＭｇと化合したＨ（キャリヤガスとしてのH_2や反応ガスであるNH_3ガスのＨが化合する）を切り離してＭｇを動き易くし、低抵抗化することができる。

【００３１】この例では、活性層７の両側をｐ型層とｎ型層の両クラッド層６、８により挟むダブルヘテロ接合構造とされ、クラッド層６、８は活性層７のバンドギャップエネルギーより大きなバンドギャップエネルギーを有する材料で構成されている。前述の$Al_xGa_yIn_{1-x-y}N$の材料でバンドギャップエネルギーを大きくするには、ｘを大きくし、１－ｘ－ｙを小さくすることによりえられる。このようなバンドギャップエネルギーを有するクラッド層６、８でサンドイッチ構造とすることにより、活性層に注入されたキャリアが発光層である活性層とクラッド層のあいだにできるエネルギー障壁で閉じ込められるため、単純な同一材料でｐｎ接合を作ったホモ接合構造より発光再結合の確立が格段に向上し、発光効率も高くなる。しかし本発明の製法はこのようなダブルヘテロ接合構造に限定されることはなく、ホモ接合やヘテロ接合のｐｎ接合でも成長する半導体層の組成を変えるだけで同様に適用される。また、半導体レーザでストライプ溝を形成することにより屈折率導波構造とする半導体発光素子なども同様に製造できる。なお、キャップ層９は電極金属１０との接触抵抗の低下のためのもので、０．２μｍ以下程度の厚さに形成される。

【００３２】つぎに、前述のように、半導体層の表面にSiO_2、Si_3N_4、Al_2O_3などの保護膜を設けて４００～８００℃で２０～６０分間程度のアニール処理を行うか、保護膜を設けないで、直接表面から３～２０ｋＶ程度の加速電圧で電子線照射をする。その結果、ｐ型層のドーパントであるＭｇとＨとの接合が切られ、活性化が達成され、ｐ型層の低抵抗化が図られる。

【００３３】ついで、Ａｕ、Ａｌなどの電極材料を蒸着やスパッタ法などにより成膜し、裏面側には全面に下部（ｎ側）電極１１が形成され、表面側はＬＥＤのばあいは発光領域を確保するため、または半導体レーザのばあいは電流注入領域を規制するため、中心部のみに残るようにパターニングして上部（ｐ側）電極１０が形成され、そののち各チップに劈開することにより、図１（ｅ）に斜視図で示されるように半導体発光素子チップが形成される。

【００３４】この半導体発光素子チップをリードフレームに載置し、ワイヤボンディングしたのちエポキシ樹脂でモールドすることによりＬＥＤが、またチップをステムに載置し、ワイヤボンディングしたのちキャップでシールすることによりレーザダイオードが完成する。

【００３５】本発明によれば、半導体単結晶基板上にチッ化ガリウム系化合物半導体層を成長させたのち、半導体単結晶基板を除去し、チッ化ガリウム系化合物半導体層を新たな基板としてその上に動作層のチッ化ガリウム系化合物半導体単結晶層を成長しているため、格子定数や熱膨張係数は非常に近くなり、格子欠陥や転位は発生しにくい。

【００３６】一方、半導体単結晶基板上に成長させた新たな基板とするチッ化ガリウム系化合物半導体層と半導体単結晶基板とのあいだの格子不整合に基因して新たな基板とするチッ化ガリウム系化合物半導体層に結晶欠陥が発生し、その結晶欠陥が動作層とするチッ化ガリウム系化合物半導体単結晶層へ広がり、転位や結晶欠陥が発生することが懸念されるが、その転位や欠陥については、その間に低温バッファ層および高温バッファ層を設けることにより有効に防止することができる。

【００３７】さらに、バッファ層とクラッド層の１μｍ以上に厚く形成される層の半導体単結晶層の組成を同じにすることにより、きれいな劈開面がえられ、鏡面がえられ易くなる。

【００３８】つぎに、さらに具体的な発光素子により本発明の製法を詳細に説明する。

【００３９】

【実施例】

実施例１

図２は本発明の製法により製造したチッ化ガリウム系ダブルヘテロ接合ＬＥＤの断面説明図である。チッ化ガリウム系化合物半導体として$Al_xGa_yIn_{1-x-y}N$（$0 \leqq x < 1$、$0 < y \leqq 1$、$0 < x+y \leqq 1$）を用い、Ａｌ、Ｇａ、Ｉｎの比率を変えることによりダブルヘテロ接合を形成したものである。

【００４０】まず、前述の図１（ｂ）に示されるような５０～２００μｍの厚さに形成されたｎ型$Al_xGa_yIn_{1-x-y}N$の半導体層からなる新たな基板とされたチッ化ガリウム系化合物半導体層基板３の表面に４００～７００℃の低温でｎ型$Al_vGa_wIn_{1-v-w}N$（$0 \leqq v < 1$、$0 < w \leqq 1$、$0 < v+w \leqq 1$、$v \leqq x$、$1-x-y \leqq 1-v-w$）からなる低温バッファ層４を０．０１～０．２μｍ程度ＭＯＣＶＤ法により成長し、ついで７００～１２００℃の高温でチッ化ガリウム系化合物半導体層基板３と同じ組成のｎ型$Al_xGa_yIn_{1-x-y}N$からなる高温バッファ層５を１～４０μｍ程度の厚さに設けた。さらに７００～１２００℃でｎ型$Al_xGa_yIn_{1-x-y}N$からなるｎ型クラッド層６を０．１～２μｍ程度の厚さに設け、ノンドープの$Al_pGa_qIn_{1-p-q}N$（$0 \leqq p < 1$、$0 < q \leqq 1$、$0 < p+q \leqq 1$、$p < x$、$1-p-q > 1-x-y$）からなる活性層７を０．０５～０．１μｍ程度の厚さに成長させ、さらにｐ型$Al_xGa_yIn_{1-x-y}N$からなるｐ型クラッド層８を１～２μｍ成長させた。その上に$Al_rGa_sIn_{1-r-s}N$（$0 \leqq r < 1$、$0 < s \leqq 1$、$0 < r+s \leqq 1$、$r \leqq x$、$1-x-y \leqq 1-r-s$）からなるキャップ層９を０．２μｍ程度の厚さ設ける。

【００４１】前記構造で、両クラッド層６、８は同じ組成で、かつ、これらの層は活性層７の組成よりバンドギャップエネルギーが大きい組成で形成されている。すなわち、Ａｌの量を多くして、Ｉｎの量を少なくすることによりバンドギャップエネルギーの大きい材料がえられ、バンドギャップエネルギーの大きい材料からなるクラッド層６、８によりバンドギャップエネルギーが小さい材料からなる活性層７がサンドイッチされる構造になっており、活性層に注入されたキャリアをエネルギー障壁で閉じ込め、発光効率を高くしている。

【００４２】そののち前述のように電子線照射によりｐ型層の低抵抗化を図り、電極を形成して劈開することにより０．５カンデラ（ｃｄ）程度の輝度のダブルヘテロ接合の青色ＬＥＤがえられた。

【００４３】本実施例によれば、バンドギャップエネルギーの小さい材料からなる活性層をサンドイッチ構造とするダブルヘテロ接合としているため、発光効率を高めることができるとともに、クラッド層やバッファ層などの厚い半導体層は同じ組成の材料で構成し、異なる組成の半導体層は結晶欠陥が生じない程度の薄さに形成されているため、欠陥のない膜質の優れた半導体層がえられ、さらに劈開が容易となる。

【００４４】実施例２

本実施例は半導体レーザ型発光素子の実施例で、各層の形成および電極の形成までは実施例１と全く同様に形成し、電極形成後に上部電極１１の両側のキャップ層９お

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よびｐ型クラッド層８の上部をエッチングしてメサ型形状にしたものである。このような構造にすることにより電流を活性層の中心部だけに集中させることができ、しかも劈開により端面が鏡面になっているため、端面で反射させて発振させることができ、出力が０．２ｍＷ程度の青色半導体レーザ型発光素子がえられた。

【００４５】実施例３

本実施例はｐｎ接合のＬＥＤの実施例で、チッ化ガリウム系化合物半導体層基板３にｎ型ＧａＮからなる低温バッファ層４を０．０１～０．２μｍ程度、ｎ型ＧａＮからなる高温バッファ層５を１～４０μｍ程度の厚さだけ実施例１と同様の条件で成長し、そののちｎ型$Al_tGa_{1-t}N$（$0 \leqq t < 1$）からなるｎ型層１２を１～２μｍ程度、ｐ型$In_uGa_{1-u}N$（$0 \leqq u < 1$）からなるｐ型層１３を０．１～０．３μｍ程度、それぞれ成膜し、ついでｐ型$Al_zGa_{1-z}N$（$0 \leqq z < 1$）からなるキャップ層１４を成膜し、ｐ型層１３に３～２０ｋＶ程度の加速電圧で電子線照射をし、アニールを行ったのち、下部（ｎ側）電極１１および上部（ｐ側）電極１０を形成し、ヘテロ接合のｐｎ接合ＬＥＤを製造した。このヘテロ接合構造とすることにより発光効率が増加し、０．２カンデラ（ｃｄ）程度の輝度の青色ＬＥＤがえられた。

【００４６】

【発明の効果】本発明によれば、基板が絶縁基板でないため、下部側の電極を基板の裏面に形成すればよく、従来のように上面側からエッチングして下部の導電型層を露出させて電極を形成する必要がない。そのため、ドライエッチング工程が不要になり、構造プロセスが簡単になるとともにエッチング時に発生しやすいコンタミネーションによる抵抗に基因する特性劣化も生じない。

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【００４７】さらに基板もクラッド層などの厚い層と同じチッ化ガリウム系化合物半導体層からなっているため、同種の結晶が揃うことになり容易に劈開することができ、簡単に鏡面をうることができる。その結果、青色の半導体レーザも容易にうることができる。

【００４８】また基板もチッ化ガリウム系化合物半導体層からなっているため、動作層と同種の半導体層であり、格子定数などが一致して格子整合がとれ、結晶欠陥や転位の発生を防止できる。その結果、半導体層が高品質になり、素子の発光効率や寿命が向上する。

【図面の簡単な説明】

【図１】本発明の半導体発光素子の製法の一実施形態の製造工程を示す図である。

【図２】本発明の製法の一実施例により製造したＬＥＤの断面説明図である。

【図３】本発明の製法の他の実施例により製造した半導体レーザの断面説明図である。

【図４】本発明の製法のさらに他の実施例により製造したＬＥＤの断面説明図である。

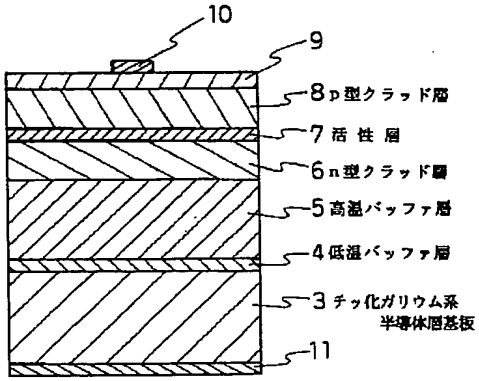
【図５】従来のＧａＮ系ＬＥＤの断面説明図である。

【図６】従来のサファイア基板上に形成されたバッファ層に発生する転位の状況を説明する図である。

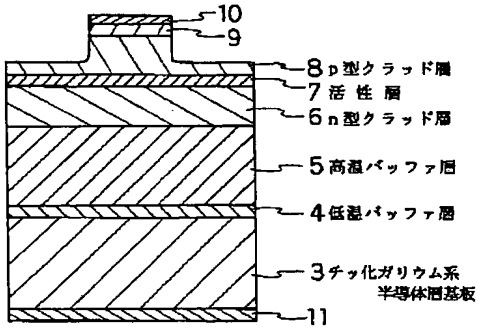
【符号の説明】

１　半導体単結晶基板
３　チッ化ガリウム系化合物半導体層基板
４　低温バッファ層
５　高温バッファ層
６　ｎ型クラッド層
７　活性層
８　ｐ型クラッド層

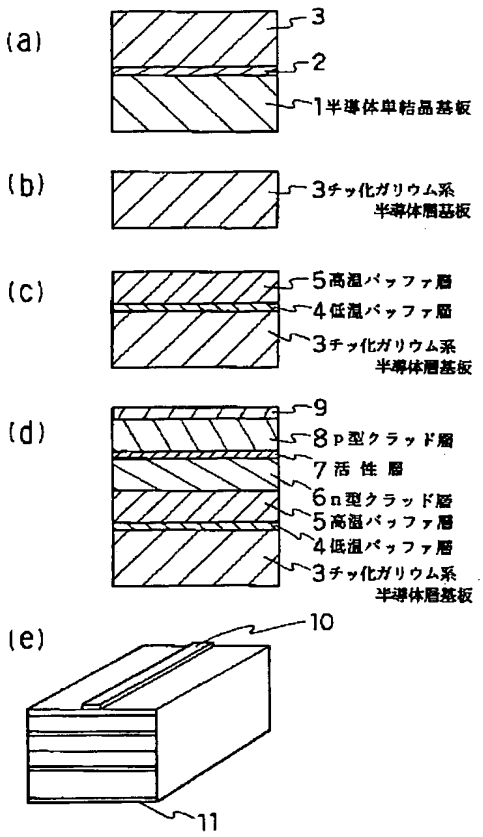
【図２】



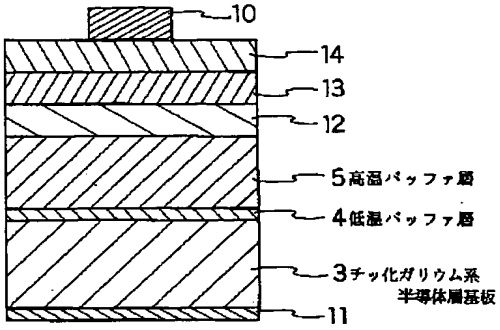
【図３】



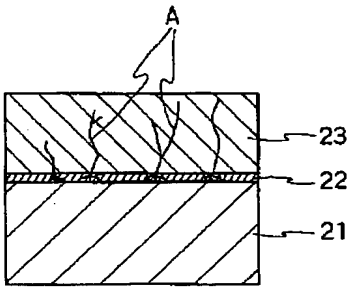
【図１】


(a)
3
2
1半導体単結晶基板
(b)
3チッ化ガリウム系
半導体層基板
(c)
5高温バッファ層
4低温バッファ層
3チッ化ガリウム系
半導体層基板
(d)
9
8p型クラッド層
7活性層
6n型クラッド層
5高温バッファ層
4低温バッファ層
3チッ化ガリウム系
半導体層基板
(e)
10
11

【図４】


10
14
13
12
5高温バッファ層
4低温バッファ層
3チッ化ガリウム系
半導体層基板
11

【図６】


A
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22
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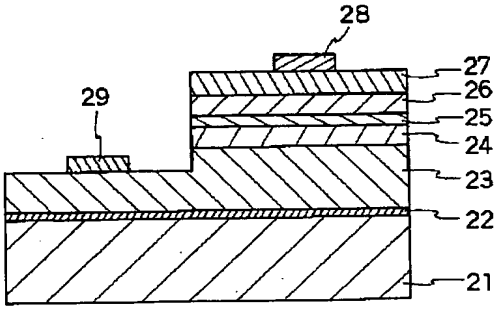
【図５】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